Customer Notification

V850E2/Px4

32-Bit Single-Chip Microcontrollers

Operating Precautions

μPD70F3506
μPD70F3507M1, μPD70F3507M2
μPD70F3508
μPD70F3509M1, μPD70F3509M2

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(A) Table of Operating Precautions

No.	Outline	μPD70 F3506	μPD70F3507		μPD70F 3508	μPD70F3509	
			M1	M2		M1	M2
	Rank[a]						
1	NEXUS interface specification is changed	appl.	appl.	appl.	appl.	appl.	appl.
2	The LVI registers are initialized after LVI reset	appl.	appl.	appl.	not appl.	not appl.	not appl.
3	PC break set to a specific instruction	appl.	appl.	appl.	not appl.	not appl.	not appl.
4	Unaligned data access crossing the upper boundary of MPU region DPA5	appl.	appl.	appl.	not appl.	not appl.	not appl.
5	Error Counter Clearing of FCN/DCN CAN controllers (Direction of use)	appl.	appl.	appl.	appl.	appl.	appl.
6	Unintended load causing RAM ECC error generation	appl.	appl.	appl.	appl.	appl.	appl.
7	Stop of AD conversion in repeat mode after start-trigger	appl.	appl.	appl.	appl.	appl.	appl.
8	Reset signal occurence and reset mask setting in debug mode	appl.	appl.	appl.	appl.	appl.	appl.
9	Software reset during data flash control sequence execution	appl.	appl.	appl.	appl.	appl.	appl.
10	Consecutive write/read access against same address in uninitialized local RAM area	appl.	appl.	appl.	appl.	appl.	appl.
11	Data Flash Tag (Direction of Use)	appl.	appl.	appl.	appl.	appl.	appl.

a. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

not appl. :Not applicable
appl.:Applicable

(B) Description of Operating Precautions

No. 1	NEXUS interface specification is changed

Details

The NEXUS interface DCUTCK frequency for MiniCube (QB-V850-EE) is specified to 20MHz.

Workaround

There is no workaround available.

No. 2	The LVI registers are initialized after LVI reset

Details

The LVI registers are set back to the reset values by the LVI reset when BIST is enabled.

Workaround

Set the LVI registers to the needed values after a reset.

No. 3	PC break set to a specific instruction

Details

If a PC break has been set to a specific instruction, the behaviour of the microcontroller is wrong. The concerned instructions and microcontroller's behaviour on PC break are:

1. HALT instruction:

- CPU will complete the operation of instruction,
- Debugger UI may hang-up,
- After release of the HALT state (if possible), PC-break will be generated and branches to Debug-Exception handler address.

2. Multiply instructions: MUL, MULH, MULHI, MULU, MAC, MACU:

- Destination register of the instruction is updated.

3. FPU instructions (see table "*Alphabetical list of concerned FPU instructions*":

- Destination register might be updated
- Floating-point system register might be updated
- Floating-point exception might be generated
- PC break is generated and branches to Debug-Exception handler address

No. 3 PC break set to a specific instruction

Alphabetical list of concerned FPU instructions:

Mnemonics	Mnemonics	Mnemonics	Mnemonics	Mnemonics
ABSF.D	CMOVF.S	CVTF.SUW	FLOORF.SUW	TRNCF.DUW
ABSF.S	CMPF.D	CVTF.SW	FLOORF.SW	TRNCF.DW
ADDF.D	CMPF.S	CVTF.ULD	MAXF.D	TRNCF.SL
ADDF.S	CVTF.DL	CVTF.ULS	MAXF.S	TRNCF.SUL
CEILF.DL	CVTF.DS	CVTF.UWD	MINF.D	TRNCF.SUW
CEILF.DUL	CVTF.DUL	CVTF.UWS	MINF.S	TRNCF.SW
CEILF.DUW	CVTF.DUW	CVTF.WD	MULF.S	
CEILF.DW	CVTF.DW	CVTF.WS	NEGF.D	
CEILF.SL	CVTF.LD	FLOORF.DL	NEGF.S	
CEILF.SUL	CVTF.LS	FLOORF.DUL	SUBF.D	
CEILF.SUW	CVTF.SD	FLOORF.DUW	SUBF.S	
CEILF.SW	CVTF.SL	FLOORF.SL	TRNCF.DL	
CMOVF.D	CVTF.SUL	FLOORF.SUL	TRNCF.DUL	

Workaround

- Renesas tool users: use latest EXEC file, where the workaround is already implemented.
- Third-party tool users: contact your tool vendor for respective solution.

No. 4	Unaligned data access crossing the upper boundary of MPU region DPA5

Details

An unaligned data access crossing the configured upper boundary of the protection region DPA5 will not be detected as an access violation.

For the DPA5 protection region the DPA5U register always specifies a “mask value” and the DPA5L register is used to specify a “base address”. These registers set the needed address range and therefore also the location of the upper boundary of this range.

If the address of an accessed data is located below the configured upper-boundary address of DPA5 and due to the length of the data, the access will cause crossing of the upper boundary - according to the present limitation an access violation will not be generated although upper bytes of the unaligned access are located beyond/above the configured upper boundary of DPA5 and an exception is expected.

Therefore it is recommended to avoid any unaligned accesses, which could lead to crossing of the upper boundary of the DPA5 region.

Please refer to V850E2M Architecture User’s Manual (U19949EJ1V0UM00) for the DPA5U and DPA5L registers description.

Workaround

There is no workaround available.

No. 5 Error Counter Clearing of FCN/DCN CAN controllers

Details

For the Px4 devices, the FCN applies.
In applications, which are clearing the error counter status during run-time, use one of the following procedure recommendations:

Notes:
1. The error counters referred to in this document are located in the registers FCNnCMINSTR, FCNnCMERCNT, DCNnCMINSTR, DCNnCMERCNT and DCNnCRERCNT.
2. The Clear Error Counter flags referred to in this document are located in the FCNnCMCLERCF/DCNnCMCLERCF/DCNnCRCLERCF bits

(1) Shutdown of CAN Module after reaching Initialization Mode

If FCN or DCN is shut down and re-started, after the initialization mode has been reached, all error counter states are cleared anyway. In addition, this also serves as a procedure to avoid any unexpected behaviour situation.
Follow the sequence below in strict order from (a) to (c).

(a) Set the FCNnGMCLCLOM / DCNnGMCLCLOM flag to clear the FCNnGMCLPWOM / DCNnGMCLPWOM global operation mode bit.

Caution: Confirm the clearance by reading back. If unsuccessful, use the forced shutdown by setting the FCNnGMCLESDE / DCNnGMCLESDE in advance.

(b) Re-start the CAN controller by setting the FCNnGMCLSEOM / DCNnGMCLSEOM bit.

Note: This leads back to initialization mode, with all error counter states cleared.

(c) Restore the register settings of the CAN module configuration.

The following register settings must be restored, because they are reset to their initial values, when the CAN module was shut down.

- FCNnGMADCTL / DCNnGMADCTL
- FCNnCMMKCTLx / DCNnCMMKCTLx
- FCNnCMCLCTL / DCNnCMCLCTL / DCNnCRCLCTL
- FCNnCMIECTL / DCNnCMIECTL / DCNnCRIECTL
- FCNnCMBRPRS / DCNnCMBRPRS / DCNnCRBRPRS
- FCNnCMBTCTL / DCNnCMBTCTL / DCNnCRBTCTL
- FCNnCMTSCTL / DCNnCMTSCTL / DCNnCRTSCTL
- DCNnCRBSSTR
- DCNnTIDRTXxH/yW
- DCNnTIDMTX0H/1H

Registers of all message buffers

Notes:
1. The interrupt status flags of FCNnCMISCTL / DCNnCMISCTL / DCNnCRISCTL are cleared and cannot be restored.

No. 5	Error Counter Clearing of FCN/DCN CAN controllers

2. The contents of the history lists are cleared and cannot be restored.
3. All message buffer contents need not to be restored, even though following flags must be cleared.

- FCNnMmCTL.FCNnMmDTNF / DCNnMmCTL.DCNnMmDTNF
- FCNnMmCTL.FCNnMmTRQF / DCNnMmCTL.DCNnMmTRQF

Please refer also to *Figure 2-1 “Shutdown and restart of CAN Module to clear Error Counters of FCN” on page 11* and *Figure 2-2 “Shutdown and restart of CAN Module to clear Error Counters of DCN” on page 12* .

(2) Clearing of all Pending Transmit Requests

Follow the sequence below in strict oder from (a) to (d).

Before entering the initialization mode of either FCN or DCN, always:

(a) Set the RXONLY_CH of the DCN to initialization mode and confirm this by reading DCNnCRCLMDOF[2:0] == 0.

Note: This is only required for DCN, if the RXONLY_CH was operated in the mirror mode.

(b) Clear any pending ABT mode trigger.

Caution: Confirm the clearance and stopping of the ABT operation by reading the FCNnGMABCTL.FCNnGMABABTT / DCNnGMABCTL.DCNnGMABABTT flag.

(c) Clear all transmit requests by software.

Cautions:
1. Any flag “FCNnMmTRQF” or “DCNnMmTRQF” must be cleared.
2. Clearing of “FCNnMmTRQF” or “DCNnMmTRQF” must be confirmed by reading back.
3. Do this also for all message buffers of the upper mirror area of DCN.

(d) Wait on transmission completion by 11 CAN bits and cleared Transmission Status Flag.

Caution: Confirm the transmission completion by waiting for 11 CAN bits and check that the transmission status flag FCNnCMCLSSTS is not set after that. This is according to a recommended transmission abort processing flow.

Please refer also to *Figure 2-3 “Clearing of Transmit Requests for FCN before clearing Error Counters” on page 13* and *Figure 2-4 “Clearing of Transmit Requests for DCN before clearing Error Counters” on page 14* .

(3) Do not clear error counters except after “bus off”

In “bus off” state, the operating precaution is not applicable. Therefore, there is no restriction in usage of the FCNnCMCLERCF / DCNnCMCLERCF, when the CAN controller is in “bus off” state.

Note: The “bus off” state can be determined by reading the FCNnCMINBOFF / DCNnCMINBOFF bit.

No. 5	Error Counter Clearing of FCN/DCN CAN controllers

(4) Do not clear the error counter states at all

According to ISO, this approach is recommended.
Like this, a node will behave according to the ISO 11898 specification. The behaviour of a node during “bus off” and the behaviour of restoring of the “error passive” state of a node are the impacts of this procedure. If the error counters are not cleared, the penalties of the ISO specification for erroneous nodes will become active, which are typically resulting in degraded performance on the CAN bus, until the node has recovered to “error active” state.

Workaround

Use one of the following procedure recommendations.

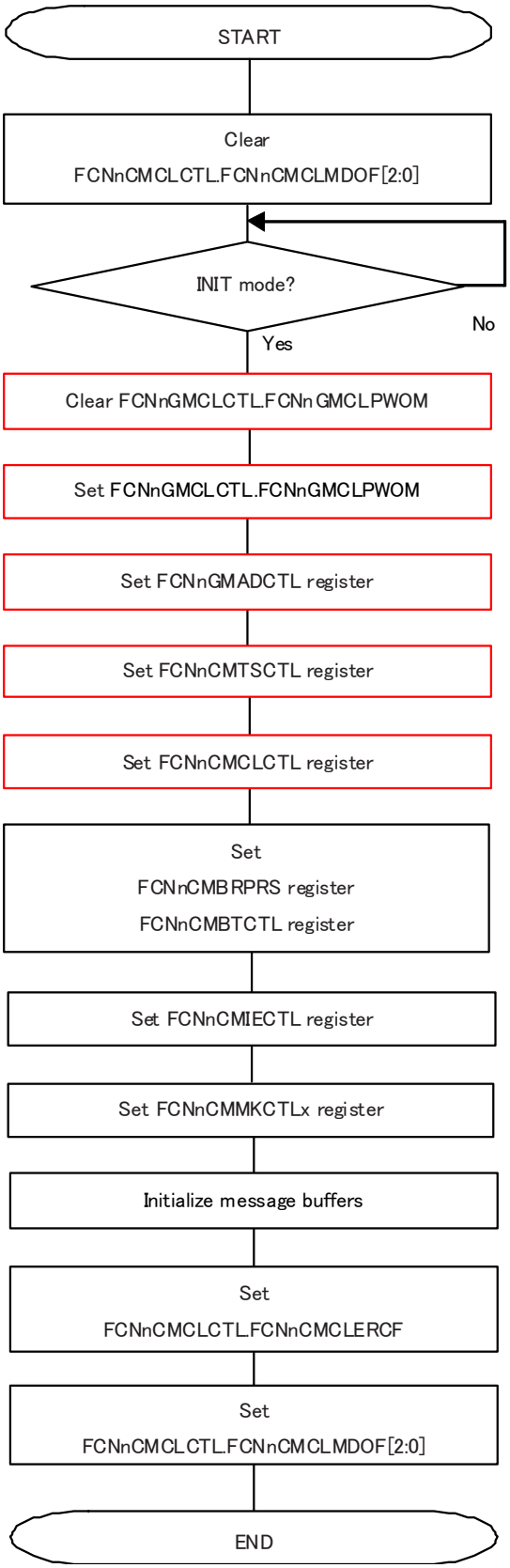

Figure 2-1 Shutdown and restart of CAN Module to clear Error Counters of FCN

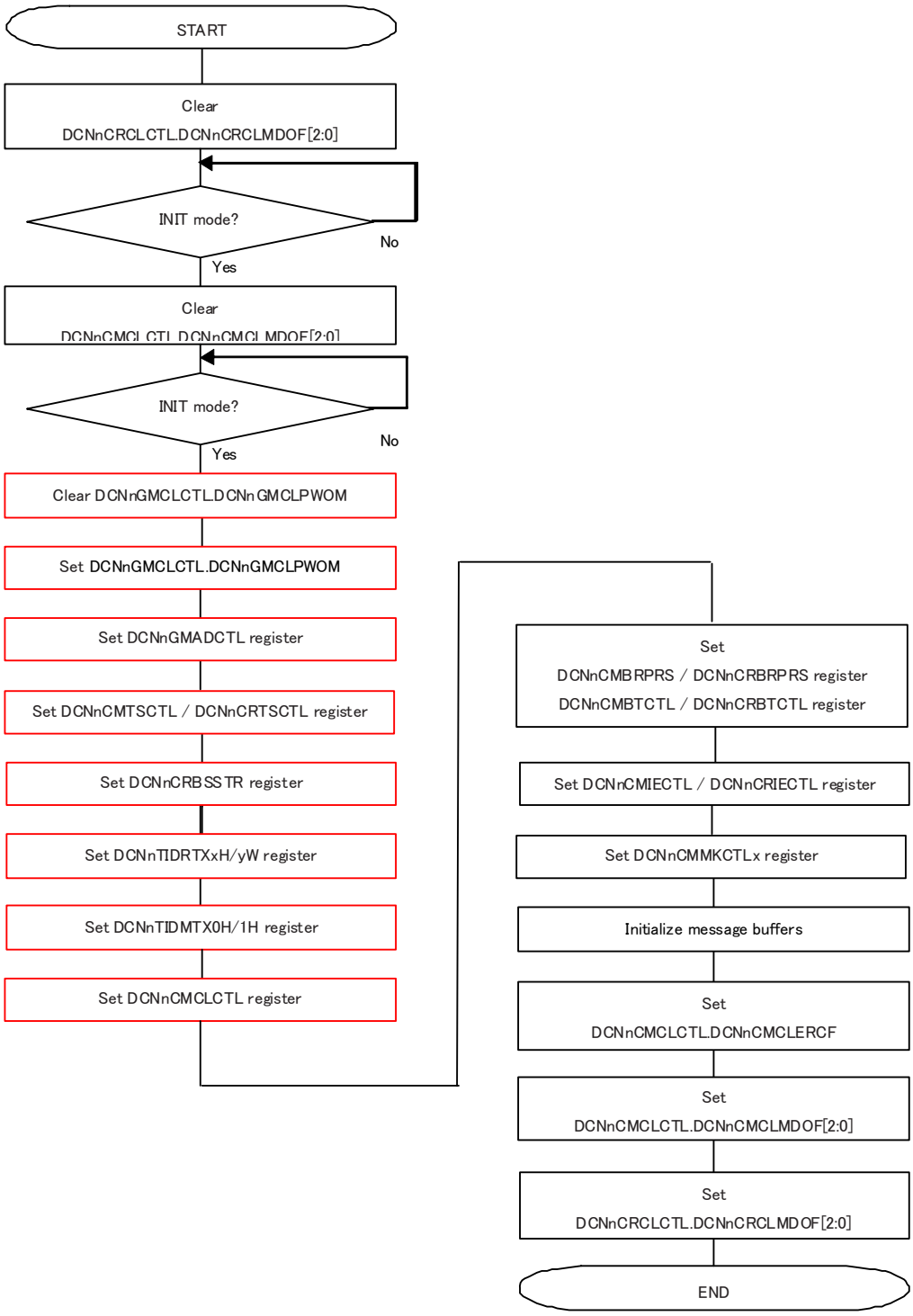

Figure 2-2 Shutdown and restart of CAN Module to clear Error Counters of DCN

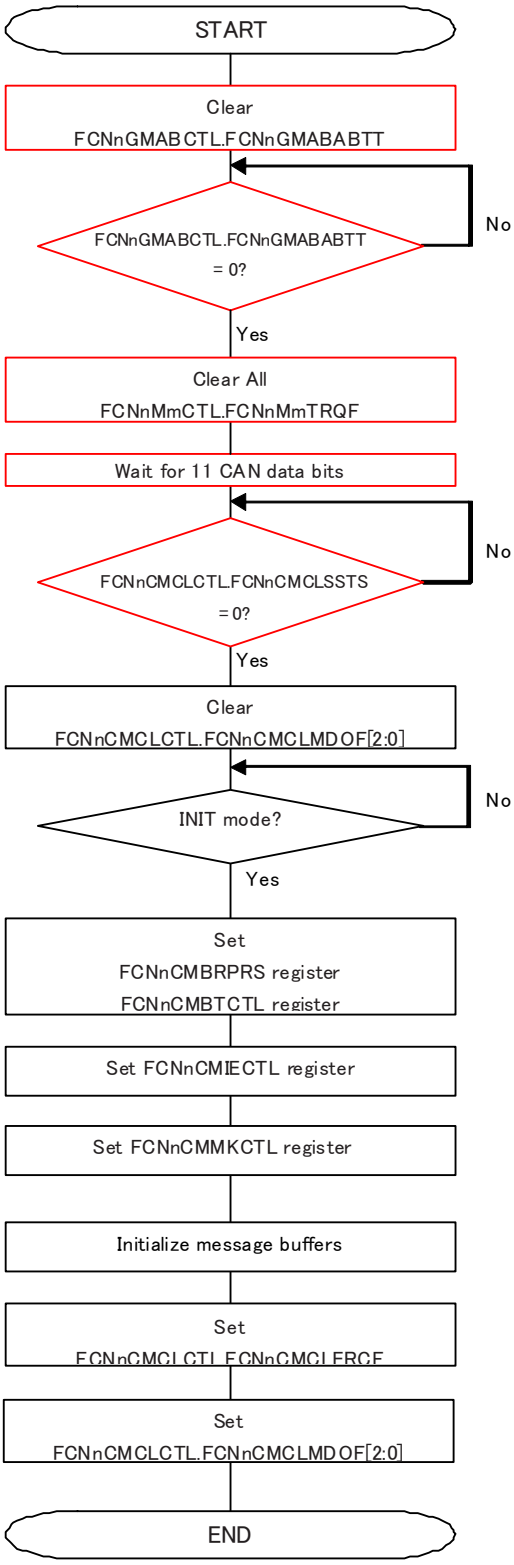

Figure 2-3 Clearing of Transmit Requests for FCN before clearing Error Counters

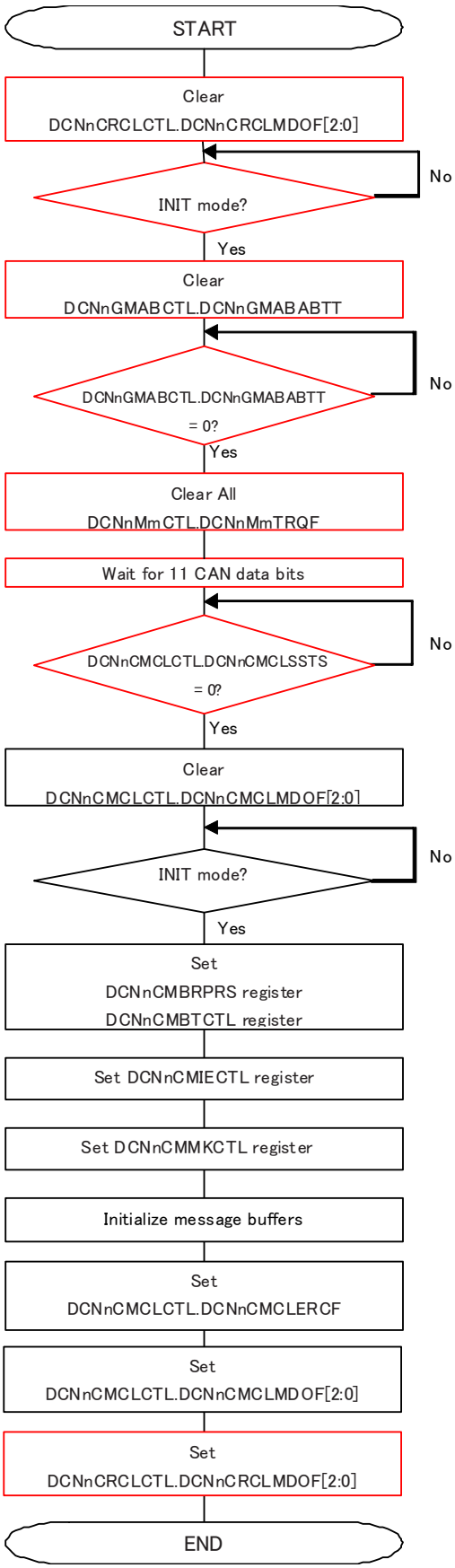

Figure 2-4 Clearing of Transmit Requests for DCN before clearing Error Counters

No. 6 Unintended load causing RAM ECC error generation

Details

An unintended load from undefined memory causes a RAM ECC error, and as a result the INTECCLRED interrupt and the SEG_FLAG.RAMF bit is set, under following conditions:

1. An instruction (no. 1), which performs the unintended read access to undefined memory, can be executed in parallel with another instruction,
2. An instruction (no. 2) before instruction no. 1 can be executed in parallel with another instruction and must perform branch/jump where the execution of instruction no. 1 is discarded (-> unintended read access).

Under these conditions an instructions combination as below may result in the unintended read access:

- Bcond, JARL, JMP or JR instruction followed by a
- LD or SLD instruction.

Instructions combinations listed below do not result in the unintended read access:

1. Any other combination of instructions do not result in the unintended read access.
   - Bit manipulation instructions or special instructions are not concerned, since these will not be executed in parallel,
   - e.g. data manipulation instructions are not concerned since these do not access any memory.
2. When the first instruction is a JARL, JMP, JR of 6 bytes length, which uses a 32-bit displacement, since these instructions will not be executed in parallel:

   JARL disp32, reg1

   JMP disp32 [reg1]

   JR disp32
3. When the LD instruction has a length of 6 bytes, which uses a 23-bit displacement, since this instruction will not be executed in parallel:

   LD.W disp23 [reg1], reg3

Workaround

One of the following workarounds can be applied.

- Avoidance of uninitialized pointers

  The unintended load from undefined memory can be avoided generally when no uninitialized pointers are used. Therefore it is recommended to initialize any pointer in a C program to an existing address, or to the NULL pointer, respectively.

No. 6	Unintended load causing RAM ECC error generation

(cont.)

- Treatment of ECC error by interrupt handler

  The memory address where the ECC error occurred can be obtained using LEDADR reister. Please add following software routine to the INTECCLRED interrupt handler:

1. read LEDADR register,
2. add offset of $FEC00000_H$ to the read value to obtain the address where error occurred,
3. if the resulting address value points to:
   - defined internal RAM. In this case the ECC error occurred at the obtained address and an error management actions have to be done,
   - undefined memory area. In this case the software routine can skip to step 4,
4. clear respective error flags in the LECCER and SGAmESSTR0 registers.

Note: If the SEG_CONT.RAME bit is enabled, consider that a SYSERR exception cannot be resumed.

No. 7	Stop of AD conversion in repeat mode after start-trigger

Details

In case a start-trigger occures during conversion end state (one ADCATCLK cycle before conversion completion) of the last channel of the last repetition in a CG repeat mode (ADCnSTM=0) the next repetitions of the conversion will be stopped.

Workaround

There is no workaround available.

No. 8	Reset signal occurence and reset mask setting in debug mode

Details

In debug mode, when an internal resset occurs and reset mask is set in the same time, the reaction on the reset signal cannot be guaranteed.

Workaround

There is no workaround available.

No. 9	Software reset during data flash control sequence execution

Details

When a software reset occurs during data flash control sequence execution, only flash related registers are initialized. This causes a difference between data flash library status (FDL) and status of data flash macro. Due to that the FDL will keep waiting on a state of the data flash until a hardware reset or Safety Guardian reset is done.

Data flash control sequence execution means a state between start of FAL_Execute function (request of Erase, Write, Write-Tag, Bit error check) and function end (return value of FAL_HAndler function is FAL_BUSY).

Workaround

If the software reset has to be done in spite of executing the data flash access, please execute a forced termination of data flash control sequence execution by FAL_Init function before issuing the software reset.

No. 10	Consecutive write/read access against same address in uninitialized local RAM area

Details

In the write path to local RAM area there is a write buffer implemented. Due to this fact and the fact, that read operation has higher priority than write operation, when a write operation to an uninitialized local RAM address is directly followed by a read operation from the same address, this read operation will result in a value read from the write data buffer, but the data under the accessed RAM address will not be changed.

If the accessed RAM address has been already initialized, the result of consecutive write/read operation will be correct. The read value and the real value under the accessed RAM address will both be correct.

Workaround

Do not execute consecutive write and read operations to the same address in the uninitialized local RAM area.

No. 11 Data Flash Tag (Direction of Use)

Details

The Data Flash of devices in UX6LF Flash technology is based on a standard 32-bit architecture. This means, that the data can be written and read in 32-bit units (read or write in 8-bit or 16-bit units is not possible). Additionally to every 32-bit data word a 33rd bit (Tag) is available for free usage.
While the 32 data bits can be read in a linear address room, the Tag can be read in another linear address room on a different address (every 32-bit address one tag can be read). The data address area starts from 0x02000000 while the Tag address area starts from 0x02100000.
Furthermore, the Tag can be written independently from the other data and it is protected against bit failures separately. The FDL provides separate functions to write the data and the tags.

Usage

The Tags are completely under control of the user application. In the EEPROM emulation library (EEL) concept, the Tag is used to write additional management data in order to ensure data consistency in case of write interruptions.
Therefore, when the EEL is applied and the MPU is adopted to protect the memory areas, the data flash tag area from 0x0210000 to 0x0217FFF has to be considered as read/write access area.

(C) Related Documents

These Operating Precautions are complementary to the following documents:

Item	Date published	Document No.	Document Title
1	July 2012	R01UH0098EJ0100	Px4 User's Manual
2	December 2009	U19949EJ1V0UM00	V850E2M Preliminary Architecture User's Manual
3	July 2010	U20280EE1V1UM00	V850 Single Voltage Flash devices with Data Flash and based on UX6LF Flash technology

(D) Revision History

Version	Date	Change description
1.0	December 2009	This is the initial version of the document.
1.1	January 2010	Corrected the name of the MiniCube tool on page 6. Updated the Related Documents sub-chapter on page 6. Modified precautions: 1, 2, 3, 6, 17. New precautions added: 5, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30.
1.2	March 2010	New precaution added: 31.
2.0	May 2010	Changed layout. Precaution 15: modified description regarding DS2.0. Precaution 17 changed to not applicable for DS1.0 and for DS2.0. Precaution 29: modified bits description. New precautions added: 32 to 41.
2.1	May 2010	Precaution 29: added correct bits description. New precaution added: 42.
2.2	July 2010	Precaution 5 is also applicable to DS1.0 devices. Precaution 17: marked as obsolete and it's description is removed from this document. A new device version has been added, please refer to chapter.
2.3	September 2010	Modified "Related Documents" chapter. DS4.0 version of the µPD70F3506 device has been included in this document. Updated precautions to include DS3.0 and DS4.0: 4, 7, 10, 15. Corrected precaution 7 regarding pseudo-error generation. Precaution 12 changed to applicable for the DS3.0 device. Updated workaround for precaution 38. New precautions added: 43, 44, 45, 46.
2.4	October 2010	New precautions added: 47, 48.
2.5	February 2011	Modified data sheet document version in the "Related Documents" chapter. DS3.1, DS4.1 and DS4.2 versions of the µPD70F3506 device have been included in this document. Updated precautions to include all device versions: 4, 7, 10, 12, 15. Corrected precaution 9. Modified description of precaution 46. New precautions added: 49, 50, 51, 52, 53.
2.51	June 2011	Modified layout of the document. Modified document number - previous version document number was: EASE-CN-0044-2.5. New precautions added: 54, 55, 56, 57, 58.
2.52	July 2011	Included information regarding µPD70F3508 device. Updated precautions to include µPD70F3508 device: 4, 7. New precautions added: 59.
2.53	August 2011	New precaution added: 60.
2.54	June 2012	Added new devices: µPD70F3507M1, µPD70F3507M2, µPD70F3509M1, µPD70F3509M2. Modified precation 8. New precautions added: 61, 62, 63, 64, 65, 66,67.

Version	Date	Change description
2.55	October 2012	Updated references table for the new User's Manual document. Removed references to the Data Sheet documents, as these are now integrated into the new User's Manual. Modified precaution 60. New precautions added: 68, 69.
3.00	December 2012	Removed all precautions, which were described in the latest User's Manual document. Please refer to the "Related Documents" chapter. Precaution #8 is applicable for all devices. Corrected list of FPU instructions in precaution #3. New precaution added: 11.

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December 19th, 2012